SWB-A31 Datasheet

Atheros AR6003 WLAN &
CSR 8810 Bluetooth Solution

REV 4

Samsung Electro-Mechanics

2011-01-21

Summary

This datasheet presents the general performance and specifications of SWB-A31 IEEE 802.11b/g/n Wireless LAN & Bluetooth V2.1+EDR/BT3.0 combination module.

Table of Contents

1 General Description

1.1 Functional Description

SWB-A31 is the combination module that integrates Wireless LAN (WLAN) and Bluetooth (BT). This embedded module is optimized for WLAN/Bluetooth enabled handheld mobile devices.

1.2 Features

- WLAN – IEEE Std 802.11b/g, 802.11n(1x1)
- Bluetooth – Bluetooth specification version 2.1 + EDR / Bluetooth 3.0
- Includes all the baseband and radio functionality, from host interface up to antenna, needs only external antenna
- Small dimensions (8.5 x 8.0 x 1.25 mm) with an LGA – 60 pin peripheral footprint
- Low power consumption
- Cellular coexistence supported
- WLAN and Bluetooth coexistence supported
- Host interfaces: SDIO for WLAN and UART, PCM for Bluetooth
- RoHS compliant
- MSL3

1.2.1 Power Management

- Supply voltage range

External power supply	V_BATT/VDD33 /PAREG_BASE	3.3V (3.14V ~ 3.46V)
	AVDD18/VREG	1.8V +/-5% (ripple Vpp<45mV)
	BT_VDD_M	3.3V (2.3V ~ 4.8V)
	BT_VDD18	1.8V (1.75V ~ 1.95V)
	SDIO & Interface Voltage	Need to meet SDIO High signal level & IO level of WLAN&BT

<Note> Users can choose between BT_VDD_M and BT_VDD18 for supplying power to BT. Refer to the Section 3.1.3.

1.2.2 Radio Transceiver

- Fully compliant with IEEE 802.11/b/g, 802.11n 1x1
- Receiver sensitivity (< 8% PER) at 11 Mbit/sec data rate: -85 dBm
- Receiver sensitivity (< 10% PER) at 54 Mbit/sec data rate: -73 dBm
- Receiver sensitivity (< 10% PER) at HT20, MCS7 : -70 dBm

- Blocking filter for suppression of CDMA, GSM, PCS and WCDMA interfering signals
- Transmitter output power in 802.11b mode: +15 dBm
- Transmitter output power in 802.11g mode at 6~36/48/54Mbps: +15/+14/+13 dBm
- Transmitter output power in 802.11n mode at HT20, MCS7: +10 dBm
- Bluetooth output power: +7 dBm (GFSK)
- Bluetooth Receiver sensitivity: -87 dBm (GFSK), -90 dBm (π/4 QPSK), -82 dBm (8DPSK)

1.2.3 Applications

- Smart phone/feature phones with embedded WLAN & Bluetooth
- Personal digital assistants (PDA) with embedded WLAN & Bluetooth
- SDIO WLAN Network Interface Cards (NIC)
- Voice over IP (VoIP) cordless phones
- Mobile gaming devices
- Portable media players (PMP) including networked MP3 player
- Networked digital camera and photo frames
- Digital media adapter and receiver
- Networked TV, set-top box, DVD recorder, personal video recorder (PVR), media drive, and other consumer electronics appliances

1.3 Block Diagram

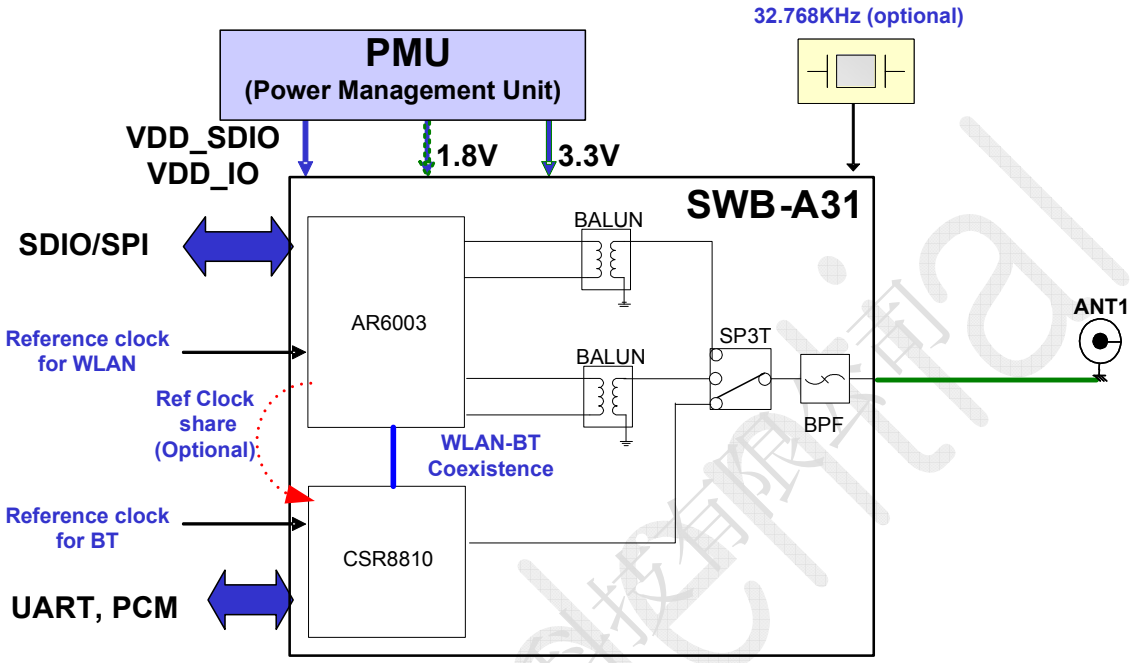


Figure 1-1 SWB-A31 hardware block diagram

2 Dimension and Pin Assignments

2.1 Mechanical Dimension

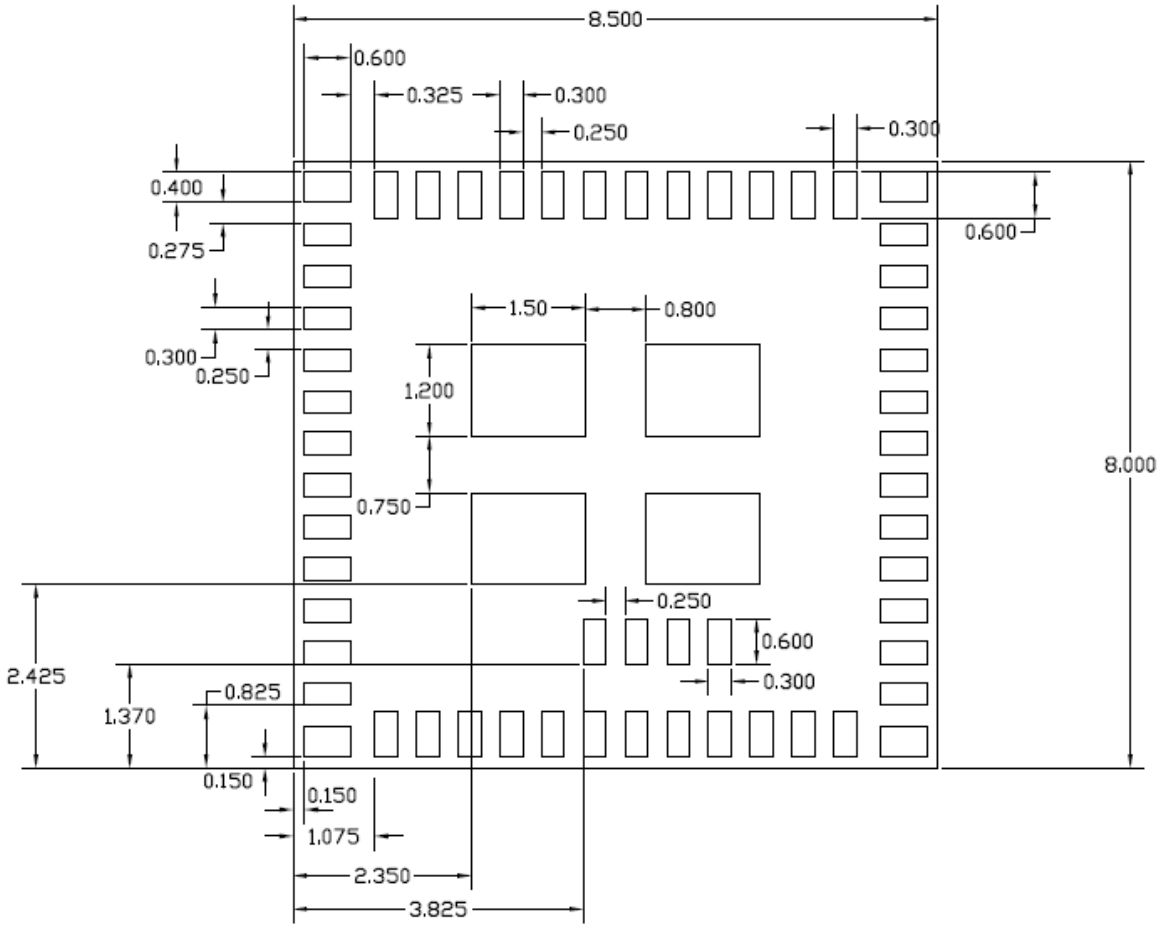


Figure 2-1 SWB-A31 Mechanical Dimension (Top View)

Parameter	Conditions	Min.	Nom.	Max.	Unit
Dimension					
X		8.4	8.5	8.6	mm
Y		7.9	8.0	8.1	mm
Height			1.25	1.35	mm

2.2 Pin Assignments

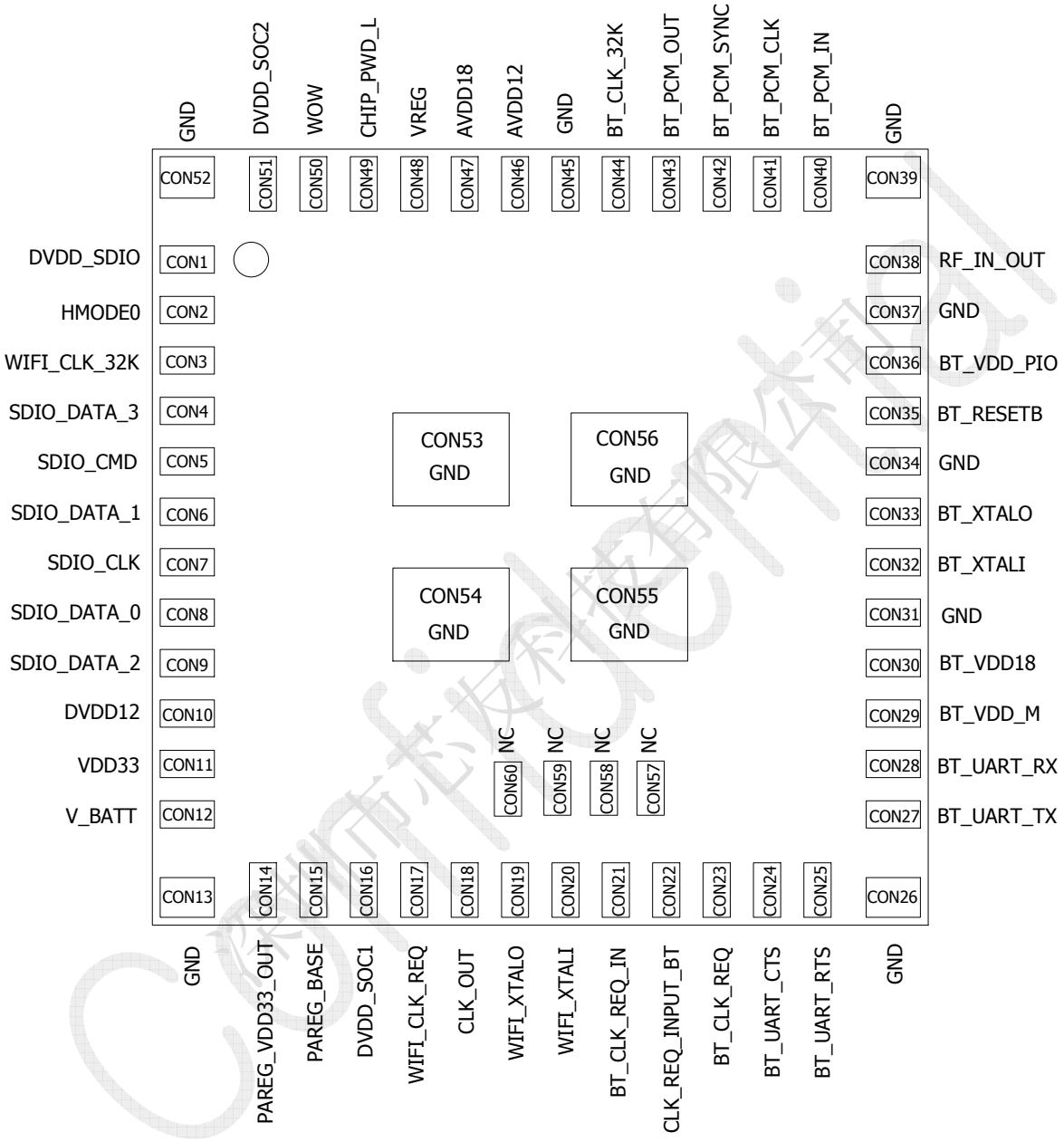


Figure 2-2 SWB-A31 Pin Assignments (Top View)

No.	Name	No.	Name	No.	Name	No.	Name
1	DVDD_SDIO	16	DVDD_SOC1	31	GND	46	AVDD12
2	HMODE0	17	WIFI_CLK_REQ	32	BT_XTALI	47	AVDD18
3	WIFI_CLK_32K	18	CLK_OUT	33	BT_XTALO	48	VREG
4	SDIO_DATA_3	19	WIFI_XTALO	34	GND	49	CHIP_PWD_L
5	SDIO_CMD	20	WIFI_XTALI	35	BT_RESETB	50	WOW
6	SDIO_DATA_1	21	BT_CLK_REQ_IN	36	BT_VDD_PIO	51	DVDD_SOC2
7	SDIO_CLK	22	CLK_REQ_INPUT_BT	37	GND	52	GND
8	SDIO_DATA_0	23	BT_CLK_REQ	38	RF_IN_OUT	53	GND
9	SDIO_DATA_2	24	BT_UART_CTS	39	GND	54	GND
10	DVDD12	25	BT_UART_RTS	40	BT_PCM_IN	55	GND
11	VDD33	26	GND	41	BT_PCM_CLK	56	GND
12	V_BATT	27	BT_UART_TX	42	BT_PCM_SYNC	57	NC
13	GND	28	BT_UART_RX	43	BT_PCM_OUT	58	NC
14	PAREG_VDD33_OUT	29	BT_VDD_M	44	BT_CLK_32K	59	NC
15	PAREG_BASE	30	BT_VDD18	45	GND	60	NC

3 Pin Descriptions

3.1 Interface, I/O, Control and Clock Pins

3.1.1 Interface, I/O, Control and Clock Pins for WLAN

Pin	Symbol	Description	Type	Circuit	Reset	Supply
SDIO Interface						
7	SDIO_CLK	SDIO input clock from HOST	I	DI	-	DVDD_SDIO
5	SDIO_CMD	SDIO command	IO	DIO		DVDD_SDIO
8	SDIO_DATA_0	SDIO data bit [0]	IO	DIO		DVDD_SDIO
6	SDIO_DATA_1	SDIO data bit [1]	IO	DIO		DVDD_SDIO
9	SDIO_DATA_2	SDIO data bit [2]	IO	DIO		DVDD_SDIO
4	SDIO_DATA_3	SDIO data bit [3]	IO	DIO		DVDD_SDIO
Antenna RF Port						
38	RF_IN_OUT	RF antenna port for 2.4G; 50Ohm (WLAN & BT)	IO	RF IO	-	-
Clock Interface						
19	WIFI_XTALO	Reference crystal output External clock source input	Crystal Output			default 26MHz
20	WIFI_XTALI	Reference crystal input	Crystal Input			default 26MHz
17	WIFI_CLK_REQ	external clock request	O	DO		VDD18_XTAL
3	WIFI_CLK_32K**	32 KHz crystal Input	I	DI	-	DVDD_SOC2
18	CLK_OUT	Reference clk output to BT chip	O			1.2V
21	BT_CLK_REQ_IN	Clock request signal from BT (for clock sharing with Bluetooth)	I	DI		DVDD_SOC1
Miscellaneous Pins						
49	CHIP_PWD_L	WiFi Reset	I	DI		DVDD_SDIO
50	WOW	wake-on-wireless(WOW)	O	DO		DVDD_SOC2
2	HMODE0	Mode configuration(For SDIO "H")	O	DO		DVDD_SOC2
No Connection Pins						
57	NC*	BT_ACTIVE	IO			DVDD_SOC1
58	NC*	WLAN_ACTIVE	IO			DVDD_SOC1
59	NC*	BT_PRIORITY	IO			DVDD_SOC1

"*" Internal use only
"**" WIFI _CLK_32K
It is possible to use internal 32KHz Clock.

3.1.2 Interface, I/O, Control and Clock Pins for Bluetooth

Pin	Symbol	Description	Type	Circuit	Reset	Circuit
UARTs Interface						
24	BT_UART_CTS	Clear to send	IO		PU	BT_VDD_PIO
25	BT_UART_RTS	Request to send	IO		PU	BT_VDD_PIO
27	BT_UART_TX	UART data transmit	IO		PU	BT_VDD_PIO
28	BT_UART_RX	UART data receive	IO		PU	BT_VDD_PIO
Antenna RF Port						
38	RF_IN_OUT	RF antenna port for 2.4G; 50Ohm (WLAN & BT)	IO	RF IO	-	-
Clock Interface						
23	BT_CLK_REQ	external X-TAL request	O		PD	BT_VDD_PIO
32	BT_XTALI	BT reference crystal input External clock source input	Crystal Input			default 26MHz
33	BT_XTALO	BT reference crystal output	Crystal Output			default 26MHz
22	CLK_REQ_INPUT_BT	BT clk_req_in for clk share	I		PD	BT_VDD_PIO
44	BT_CLK_32K**	32 KHz crystal Input	I		PD	BT_VDD_PIO
PCM Interface						
40	BT_PCM_IN	PCM data input from host or codec	I		PD	BT_VDD_PIO
42	BT_PCM_SYNC	PCM synchronous data strobe	IO		PD	BT_VDD_PIO
41	BT_PCM_CLK	PCM synchronous data clock	IO		PD	BT_VDD_PIO
43	BT_PCM_OUT	PCM data output to host or codec	O		PD	BT_VDD_PIO
Miscellaneous Pins						
35	BT_RESETB	BT Reset	I	-	PD	BT_VDD_PIO
No Connection Pins						
60	NC*	SPI_PCM_SEL	IO		PD	BT_VDD_PIO

"*" Internal use only
"**" BT_CLK_32K
When the BT uses a crystal oscillator, an external sleep clock is not required.

"Type" Column : I=Input, O=Output, IO=Bi-directional

3.1.3 Power and Ground Pins

Pin	Symbol	Description	Min.	Nom.	Max.	Unit
WLAN power pins						
46	AVDD12	Just connect 2.2uF capacitor		-		
10	DVDD12	Just connect 2.2uF capacitor		-		
47	AVDD18	Analog 1.8V supply Provides power to analog baseband and RF blocks	1.71	1.8	1.89	V
16	DVDD_SOC1	GPIO Supply voltage Provides power for BT-coexistence & the CLK_REQ signal	1.71		3.46	V
51	DVDD_SOC2	GPIO Supply voltage Provides power for external sleep clock input, JTAG, UART,HMODE and WoW	1.71		3.46	V
1	DVDD_SDIO	SDIO Interface Voltage Provides power for SDIO host interface	1.71		3.46	V
11	VDD33	3.3V supply for EPA & Antenna control I/O supply	3.14	3.3	3.46	V
48	VREG	Digital 1.8V supply Provides power to internal 1.2V regulators	1.71	1.8	1.89	V
15	PAREG_BASE	PAREG input	3.14	3.3	3.46	V
14	PAREG_VDD33_OUT	Just connect 2.2uF or 4.7uF capacitor		-		V
12	V_BATT		3.14	3.3	3.46	V
BT Power Pins						
29	BT_VDD_M*	Input to internal high voltage regulator	2.3	3.3	4.8	V
30	BT_VDD18**	Output from internal high voltage regulator and Input to internal low voltage regulator	1.75	1.8	1.95	V
20	BT_VDD_PIO	BT IO Level (Meet to BT – UART , BT – PCM Level BT – Coexistence IO Level)	1.2		3.6	V
GND Pins						
13	GND	Ground				-
26	GND	Ground				-
34	GND	Ground				-
37	GND	Ground				-
39	GND	Ground				-
45	GND	Ground				-
52	GND	Ground				-
53	GND	Ground				-
54	GND	Ground				-
55	GND	Ground				-
56	GND	Ground				-

"*" BT_VDD_M pin is input to internal high voltage regulator.
The high voltage regulator generates the main 1.8V
When this regulator is not used, BT_VDD_M pin must be left unconnected or tied to BT_VDD18

"**" BT_VDD18 pin is output from internal high voltage regulator and input to internal low voltage regulator.
When the power is supplied to BT_VDD_M by external power source, this pin must be unconnected.

4 Electrical Characteristics

4.1 DC Characteristics

4.1.1 Absolute Maximum Ratings

Symbol(Domain)	Parameter	Max Rating	Unit
WLAN			
VREG	Digital 1.8V supply	-0.3 to 2.5	V
AVDD18	Analog 1.8V supply	-0.3 to 2.5	V
DVDD_SDIO	SDIO I/O supply	-0.3 to 4.0	V
DVDD_SOC1	GPIO I/O supply	-0.3 to 4.0	V
DVDD_SOC2	GPIO I/O supply	-0.3 to 4.0	V
VDD33	3.3V supply for EPA	-0.3 to 4.0	V
PAREG_BASE	PAREG input	-0.3 to 4.0	V
V_BATT		-0.3 to 4.0	V
BT			
BT_VDD_PIO	IO supply for BT	-0.4 to 3.6	V
BT_VDD18	Output from internal high voltage regulator and Input to internal low voltage regulator	1.7 to 2.0	V
BT_VDD_M	Input to internal high voltage regulator	2.3 to 4.8	V

4.1.2 Recommended Operating Conditions

Symbol(Domain)	Parameter	Min.	Nom.	Max.	Unit
WLAN					
VREG	Digital 1.8V supply	1.71	1.8	1.89	V
AVDD18	Analog 1.8V supply	1.71	1.8	1.89	V
DVDD_SDIO	SDIO I/O supply	1.71		3.46	V
DVDD_SOC1	GPIO0 I/O supply	1.71		3.46	V
DVDD_SOC2	GPIO1 I/O supply	1.71		3.46	V
VDD33	3.3V supply	3.14	3.3	3.46	V
PAREG_BASE	PAREG input	3.14	3.3	3.46	V
V_BATT		3.14	3.3	3.46	V
BT					
BT_VDD_PIO	BT – Coexistence IO Level (Meet to WLAN IO level)	1.2		3.6	V
BT_VDD18	1.8V supply	1.75	1.8	1.95	V
BT_VDD_M	Input to internal high voltage regulator	2.3	3.3	4.8	V

4.2 Power Consumption

4.2.1 Current consumption at WLAN

Parameter	Conditions	Min.	Nom.	Max.	Unit
Tx mode (11b Max current)					
1.8V*	15dBm @11Mbps		61		mA
IO Part***			211		mA
3.3V**					mA
Tx mode (11g Max current)					
1.8V*	13dBm @54Mbps		66		mA
IO Part***			132		mA
3.3V**					mA
Tx mode (11n Max current)					
1.8V*	10dBm @HT20, MCS7		67		mA
IO Part***			106		mA
3.3V**					mA
Rx mode					
1.8V*	Rx @Max gain		75		mA
IO Part***			5		mA
3.3V**					mA
Sleep mode					
1.8V*			0.21		mA
IO Part***			0.005		mA
3.3V**					mA

"*" VREG, AVDD18
"**" VDD33, PAREG_BASE,PAREG_VDD33_OUT,V_BATT
"***" DVDD_SOC1, DVDD_SOC2, DVDD_SDIO (Supplied 3.3V for testing power consumption)

4.2.2 Bluetooth Current Consumption

Parameter	Conditions	Min.	Nom.	Max.	Unit
SCO	Master HV3		15		mA
	Slave HV3		17		mA
ACL Data transfer	Master-Tx DH1 (@7dBm)		27		mA
	Slave-Rx DH1 (@7dBm)		28		mA
Sniff mode	Master ACL connection 1.28s interval		0.46		mA
	Slave ACL connection 1.28s interval		0.48		mA
Scans	Inquiry scan 1.28s		0.40		mA
	Page scan 1.28s		0.46		mA
	Inquiry scan 1.28 & Page scan 1.28s		0.84		mA
Sleep			0.15		mA

4.3 Environmental Characteristics

Symbol	Parameter	Conditions	Min.	Max.	Unit
ESD	Electro-static discharge voltage	HBM		Class 1C	V
T_{OP}	Operating temperature		-20	70	°C
T_{STG}	Storage temperature		-30	85	°C

5 RF Specifications

All measurements are made under nominal supply voltage and room temperature conditions.

5.1 WLAN Receiver RF Specifications

Parameter	Conditions	Min.	Nom.	Max.	Unit
Minimum receiver sensitivity in 802.11b mode					
1Mbps	PER<8%, Packet size= 1024bytes			-80	dBm
2Mbps				-80*	dBm
5.5Mbps				-76	dBm
11Mbps			-85	-76*	dBm
Minimum receiver sensitivity in 802.11g mode					
6Mbps	PER<10%, Packet size= 1000bytes			-82*	dBm
9Mbps				-81*	dBm
12Mbps				-79*	dBm
18Mbps				-77*	dBm
24Mbps				-74*	dBm
36Mbps				-70*	dBm
48Mbps				-66*	dBm
54Mbps			-73	-65*	dBm
Minimum receiver sensitivity in 802.11n mode					
HT20, MCS7, 1stream, 1Tx, 1Rx	PER<10%		-70	-64*	dBm
Maximum input signal level					
802.11b mode	PER<8%	-10*			dBm
802.11g mode	PER<10%	-20*			dBm
802.11n mode	PER<10%	-20*			dBm
Adjacent channel rejection (ACR) in 802.11b mode					
1Mbps	PER<8%, Packet size= 1024bytes	35*			dB
2Mbps		35*			dB
5.5Mbps		35*			dB
11Mbps		35*			dB
Adjacent channel rejection (ACR) in 802.11g mode					
6Mbps	PER<10%, Packet size= 1024bytes	16*			dB
9Mbps		16*			dB
12Mbps		13*			dB
18Mbps		11*			dB
24Mbps		8*			dB

36Mbps		4*			dB
48Mbps		0*			dB
54Mbps		-1*			dB
Adjacent channel rejection (ACR) in 802.11n mode					
HT20, MCS0	PER<10%	16*			dB
HT20, MCS7		-2*			dB

"*" indicates IEEE 802.11 standard specifications

5.2 WLAN Transmitter RF Specifications

Parameter	Conditions	Min.	Nom.	Max.	Unit
Linear output power in 802.11b mode					
Output power@1~11Mbps	As specified in IEEE802.11		15		dBm
Linear output power in 802.11g mode					
Output power@6~36Mbps	As specified in IEEE802.11		15		dBm
Output power@48Mbps			14		dBm
Output power@54Mbps			13		dBm
Linear output power in 802.11n mode					
Output power@HT20,MCS7			10		dBm
Transmit spectrum mask					
Margin to 802.11b spectrum mask	Maximum output power	0	5		dBr
Margin to 802.11g spectrum mask		0	5		dBr
Margin to 802.11n spectrum mask		0	5		dBr
Transmit modulation accuracy in 802.11b mode					
1Mbps	As specified in IEEE802.11b	-		35	%
2Mbps		-		35	%
5.5Mbps		-		35	%
11Mbps		-		35	%
Transmit modulation accuracy in 802.11g mode					
6Mbps	**Mandatory**	**-**		**-5**	**dB**
9Mbps	Option	-		-8	dB
12Mbps	**Mandatory**	**-**		**-10**	**dB**
18Mbps	Option	-		-13	dB
24Mbps	**Mandatory**	**-**		**-16**	**dB**
36Mbps	Option	-		-19	dB
48Mbps	Option	-		-22	dB
54Mbps	Option	-	-29	-25	dB
Transmit modulation accuracy in 802.11n mode					
HT20,MCS7			-30	-28	dB
Transmit power-on and power-down ramp time in 802.11b mode					
Transmit power-on ramp time from 10% to 90% output power				2	usec
Transmit power-down ramp time from 90% to 10% output power				2	usec

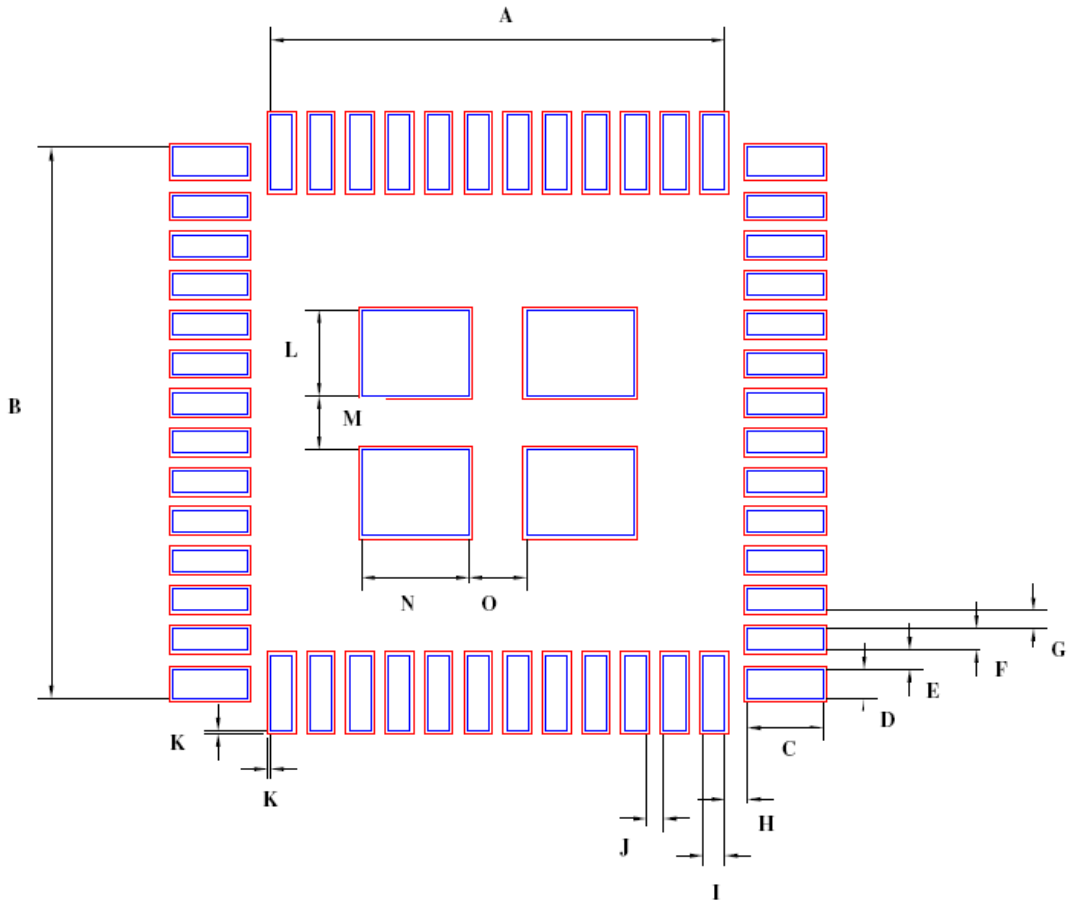
5.3 Bluetooth RF Specifications

Parameter		Conditions	Min.	Nom.	Max.	Unit
Output power*		CLASS1	0	7	20	dBm
		CLASS2	-6		4	
Frequency range			2402		2480	MHz
ICFT (Initial Carrier Frequency Tolerance)			-75		75	kHz
Carrier frequency drift	DH1		-25		25	kHz
	DH3		-40		40	kHz
	DH5		-40		40	kHz
	Maximum drift rate		-20		20	kHz/50us
Modulation characteristics	Delta f1 avg		140		175	kHz
	Delta f2 max		115			kHz
	Delta f2 avg/delta f1 avg		80		-	%
Sensitivity (GFSK, BER<=0.1%)				-87	-70	dBm
EDR relative power			-4		1	dBm
EDR modulation accuracy	RMS DEVM, $\pi/4$ DQPSK		0.0		0.20	-
	RMS DEVM, 8DPSK		0.0		0.13	-
	Peak DEVM, $\pi/4$ DQPSK		0.0		0.35	-
	Peak DEVM, 8DPSK		0.0		0.25	-
EDR Sensitivity ($\pi/4$ DQPSK , BER<=0.01%)			-	-90	-70	dBm
EDR Sensitivity (8DPSK , BER<=0.01%)			-	-82	-70	dBm

" *" Output power adjustment in SWB-A31 - All BT RF performances are measured with script offered by SEMCO. Script is optimized SWB-A31. So if different value is used, SEMCO can't guarantee all BT RF performance .

6 Assembly Recommendations

6.1 Printed Circuit Board and Stencil Design

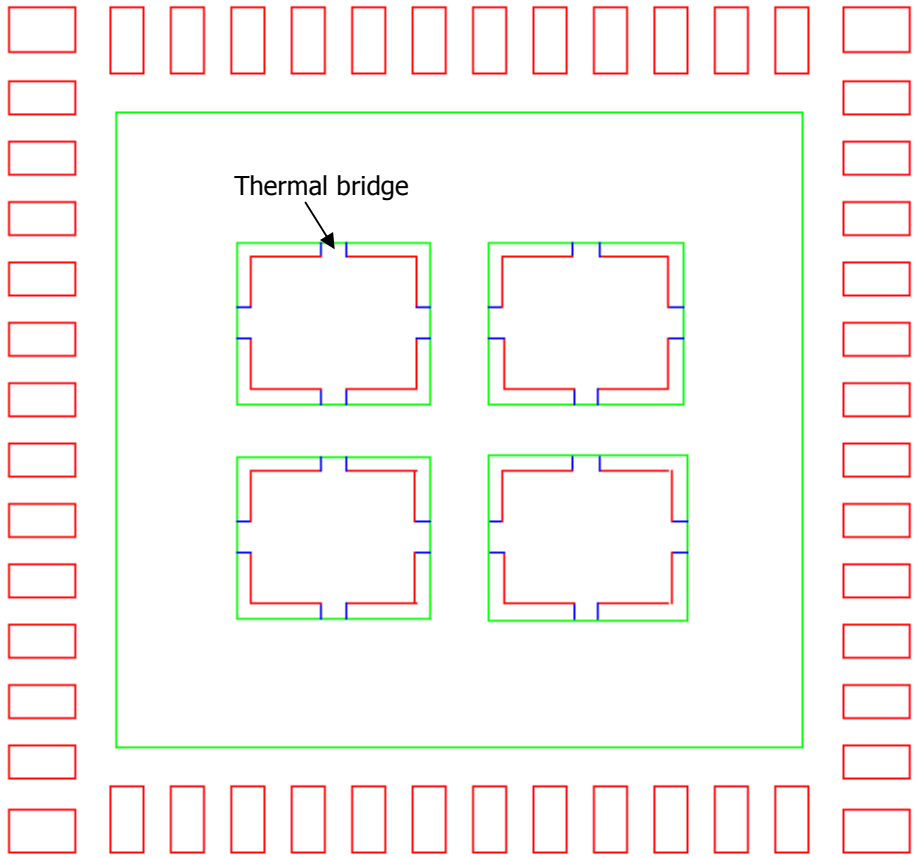


	Nom.	Unit	Dimension	Nom.	Unit
A	6.350	mm	I	0.300	mm
B	7.700	mm	J	0.250	mm
C	1.050	mm	K	0.050	mm
D	0.400	mm	L	1.200	mm
E	0.275	mm	M	0.750	mm
F	0.300	mm	N	1.500	mm
G	0.250	mm	O	0.800	mm
H	0.325	mm			

* Note
Land: **Blue** Color
SR Open: **Red** Color
Metal Mask Open Size = Land Size(Customer needs to modify based on their production line)

<Example>

SEMCO recommend users to make thermal bridge for the best soldering as below



* Note
Thermal Bridge: Blue Color, Land: Red Color, SR: Green Color

6.1.1 PCB Finish

The SWB-A31 can be mounted on a variety of PCB finishes such as immersion gold (Ni/Au) or Hot air solder level (HASL) or Organic Surface Protection (OSP).

Ni/Au finish is recommended. OSP is not recommended in cases that OSP does not withstand a Pb-free or a double-sided reflow application.

6.2 Solder Paste

Standard (No-clean) Sn/Pb (63%/37%) or Pb-free solder pastes should be used for soldering the package. Solder pastes should be selected based on their printing and reflow behavior. For Pb-free solder paste it is recommended to use "SAC" type solder paste (e.g. SnAg3.8Cu0.7) with melting point of 217°C.

6.3 Reflow Profile

Industrial convection reflow oven should be used to mount the packages. The profile depends on the printed circuit board and other components that are used in the customer application. For maximum peak temperature JEDEC specification should be followed. Following re-flow profile and constraints are recommended for eutectic Sn/Pb and Pb-free reflow solders

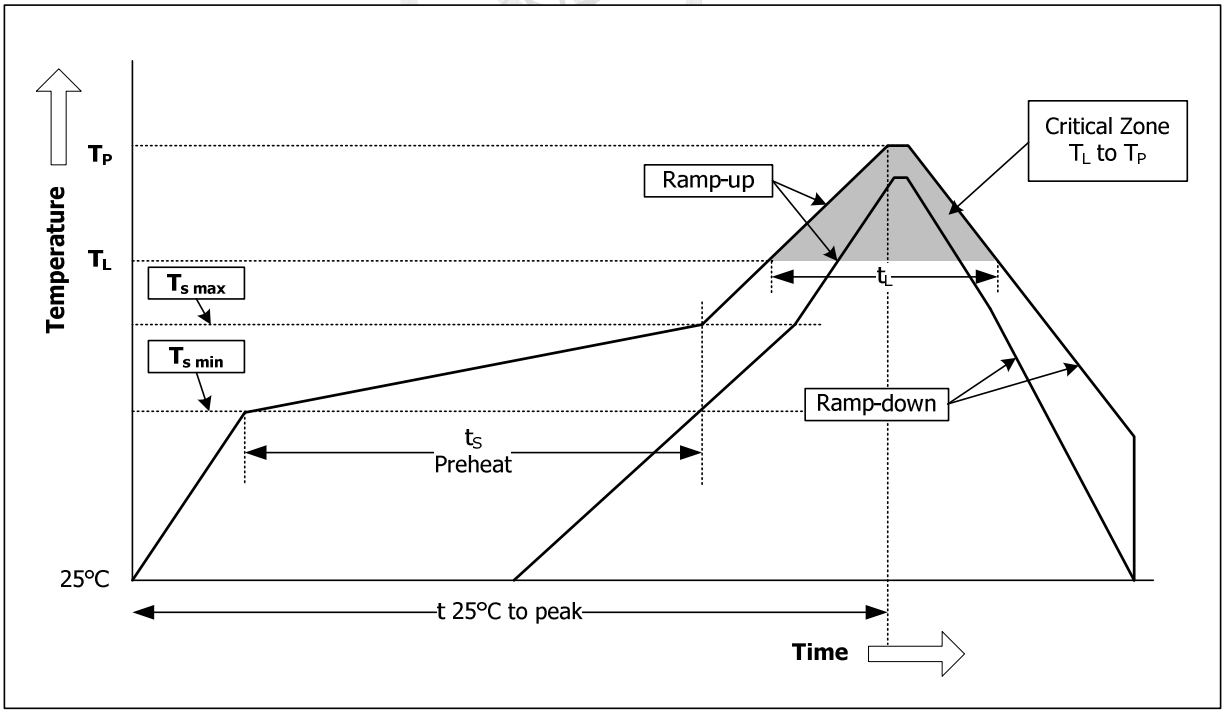


Figure 6-1 Recommended Reflow Temperature Profile

	Eutectic Sn/Pb	Pb-free
Average ramp-up rate (T_{Smax} to T_p)	2°C /second max	2°C /second max
Preheat		
-Temperature Min(T_{Smin})	100 °C	150 °C
-Temperature Max(T_{Smax})	150 °C	200 °C
-Time(T_{Smin} to T_{Smax})	60-120 seconds	75-90 seconds(≤0.75℃/second)
Time maintained above:		
-Temperature(T_L)	183 °C	217 °C
-Time(t_L)	60-90 seconds	70-90 seconds
Max. Peak Temperature(T_p)	240 +/-5 °C	255 ± 5 °C (max 260°C)
Time within 5℃ of actual Peak Temperature(t_P)	10-30 seconds	20-30 seconds
Ramp-Down Rate	>180°C: 2 °C /second max. <180°C: 6 °C /second max.	>180°C: 2 °C /second max. <180°C: 6 °C /second max.
Minimum Peak Temperature(Tp_{min})	205 °C	230 °C
Time 25 °C to Tp	4-5 minutes	4-5 minutes

* Lead free devices will withstand up to 3 reflow to a maximum temperature of 255℃ for 10 seconds

7 Additional Information

7.1 Host Interface Configurations

7.1.1 WLAN Mode setting

HMODE0	Configuration
High (DVDD_SOC2)	SDIO Mode
GND	GSPI Mode

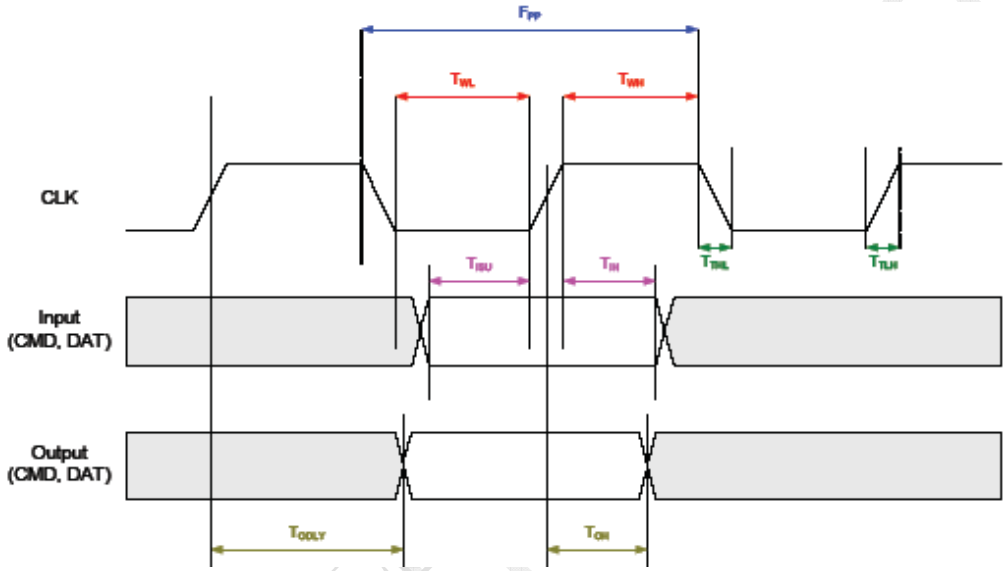


Figure 7-1 SDIO 2.0 timing

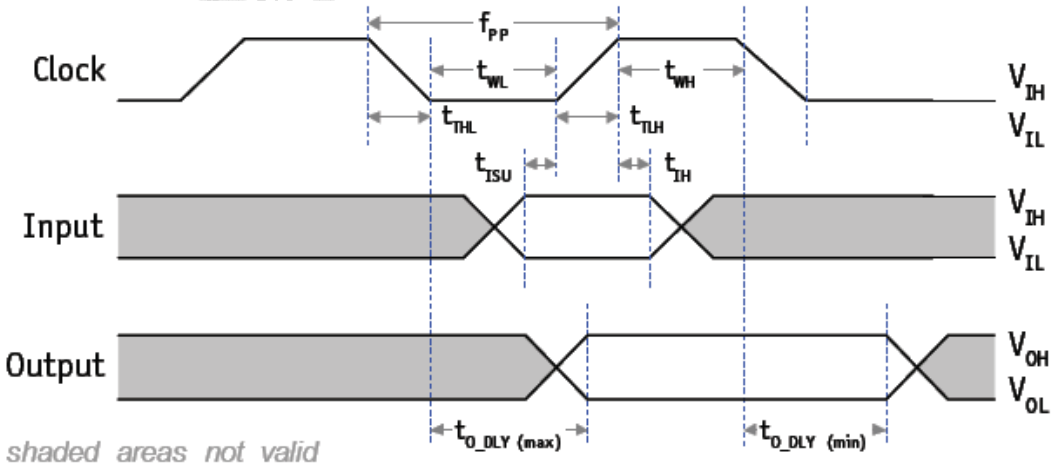


Figure 7-2 GSPI timing

SDIO Timing Constraints

Parameter	Description	Min.	Max.	Unit	Note
f_{PP}	Clock frequency data transfer mode	0	50	MHz	40pF ≥ C_L
t_{WL}	Clock low time	7	-	ns	40pF ≥ C_L
t_{WH}	Clock high time	7	-	ns	40pF ≥ C_L
t_{TLH}	Clock rise time	-	10	ns	40pF ≥ C_L
t_{THL}	Clock fall time	-	10	ns	40pF ≥ C_L
t_{ISU}	Input setup time	6	-	ns	40pF ≥ C_L
t_{IH}	Input hold time	2	-	ns	40pF ≥ C_L
t_{OH}	Output hold time	2.5	-	ns	40pF ≥ C_L
$t_{O\_DLY\ (min)}$	Output delay time during data transfer mode	0	14	ns	40pF ≥ C_L

GSPI Timing Constraints

Parameter	Description	Min.	Max.	Unit	Note
f_{PP}	Clock frequency	0	48	MHz	
t_{WL}	Clock low time	8.3	-	ns	
t_{WH}	Clock high time	8.3	-	ns	
t_{TLH}	Clock rise time	-	2	ns	
t_{THL}	Clock fall time	-	2	ns	
t_{ISU}	Input setup time	5	-	ns	
t_{IH}	Input hold time	5	-	ns	
t_{O_DLY}	Output delay	0	5	ns	

7.1.2 Bluetooth

Interface : UART

Four signals are used to implement the UART function.

UART_RX and UART_TX transfer data and UART_CTS and UART_RTS can be used to implement RS232 hardware flow control where both are active low indicators.

The interface consists of four-line connection as described in below :

Signal name	Driving source	Description
UART_TX	SEMCO module	Data from SEMCO module
UART_RX	Host	Data from Host
UART_RTS	SEMCO module	Request to send output of SEMCO module
UART_CTS	Host	Clear to send input of SEMCO module

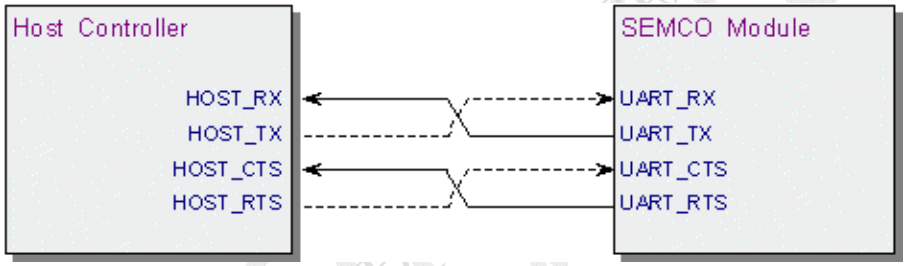


Figure 7-3 The Example for Bluetooth UARTs Interface Connection

Possible UART Settings

Bluetooth Module can handle UART baudrate from 9.6kbps up to 4Mbps.

UART configuration parameters, such as baud rate and packet format, are set using CSR8810 firmware.

However, host shall communicate with default setting UART connection initiated at first time.

Property	Possible Values
Baud rate	Min 9600 Baud, Max 4M Baud (≤1% Error)
Flow Control	RTS/CTS or None
Bits per byte	8
Parity	None, Odd or Even
Number of Stop Bits	1 or 2

Interface : PCM

Bluetooth Function offers a bi-directional digital audio interface that routes directly into the baseband layer of the on-chip firmware. It does not pass through the HCI protocol layer. It allows the data to be sent to and received from a SCO connection.

This interface consists of four signals : a clock(PCM_CLK), a data input(PCM_IN), a data output (PCM_OUT), and a frame-synchronization signal(PCM_SYNC)

Possible PCM settings

Bluetooth Function can operate as the PCM interface master generating an output clock of 128, 256, 512, 1536 or 2400kHz.

When configured as a PCM interface slave, it can operate with an input clock up to 2400kHz.

Property	Possible Values
Mode	Slave, Master
Clock rate	Master mode : 128, 256, 512, 1536, 2400kHz Slave mode : Up to 2400kHz
Clock formats	Long Frame Sync, Short Frame Sync, GCI timing environment
Sample formats	13 or 16-bit linear, 8-bit u-law or A-law

7.2 Power On/Off Sequences

7.2.1 Power On/Off Sequences for WLAN

The following two figures show the recommended power up/down and reset sequences for the AR6003 using external 3.3V and 1.8V supplies.

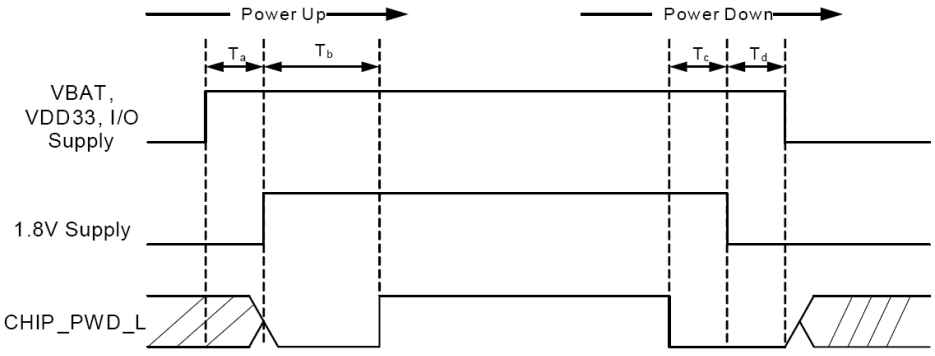


Figure 7-4 Power-Up/Power-Down Timing

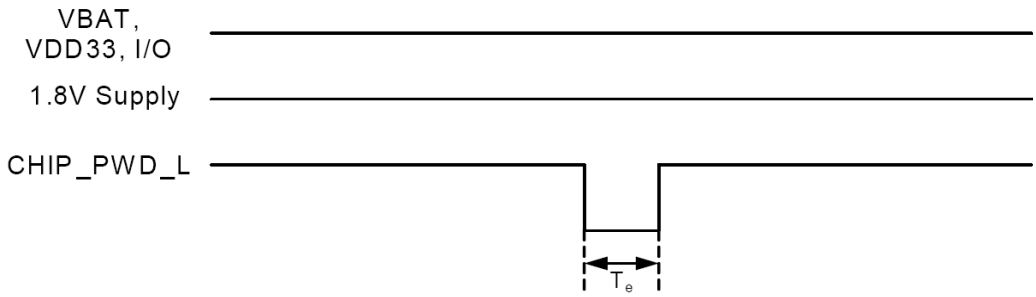


Figure 7-5 Reset and Power Cycle Timing

Symbol	Descriptions	Min. (usec)
Ta	Time between V_BATT, VDD33, and I/O supplies valid and 1.8V supply valid	0
Tb	Time between 1.8V supply valid and CHIP_PWD_L deassertion	5
Tc	Time between CHIP_PWD_L assertion and 1.8V supply invalid	0
Td	Time between 1.8V supply invalid and V_BATT, VDD33, and I/O supplies invalid	N/A
Te	Length of CHIP_PWD_L pulse	5

Table 7-1 Timing Diagram Definitions

*** Note**
1.8V Supply: VREG, AVDD18
VBATT,VDD33 Supply: V_BATT,VDD33,PAREG_BASE
I/O Supply: DVDD_SDIO, DVDD_SOC1, DVDD_SOC2

7.2.2 Power On Sequences for Bluetooth

Bluetooth does not have any strict relative timing requirements for clock and power supply sequencing during reset or power_on. Following this sequence of operation to ensure that the initial cold boot is completed successfully;

1. All external power supplies should be stable and the sleep clock should be present.
2. BT_RESETB should be driven high.
3. The external reference clock must be present and stable a variable number of milliseconds after the Bluetooth asserts its clock request signal. The default value is 5ms.

It is then possible to establish host communications with the Bluetooth in order to set further configuration values. When you have set configuration values, perform a warm reset so that they take effect and normal radio operation can begin.

7.2.3 Reset for Bluetooth

Bluetooth the reset function is internally tied to the BT_RESETB pin. Bluetooth may be reset from several sources;

1. BT_RESETB pin
2. Power on reset
3. A UART break character
4. Via a software-configured watchdog timer

The BT_RESETB pin is an active low reset. To ensure a full reset the rest signal should be asserted for a period greater than 5ms.

A warm reset function is also available under software control. After a warm reset the RAM data remains available.

7.3 Reference and Sleep Clock Requirements

7.3.1 Sleep Clock for WLAN

The SWB-A31 does not require an external 32KHz clock for WLAN. By default, the SWB-A31 will utilize its internal 32KHz clock. If a more accurate 32KHz clock is needed, then it can be supplied externally via the WIFI_CLK_32K pin. The WIFI_CLK_32K input clock timing and voltage requirements are shown below.

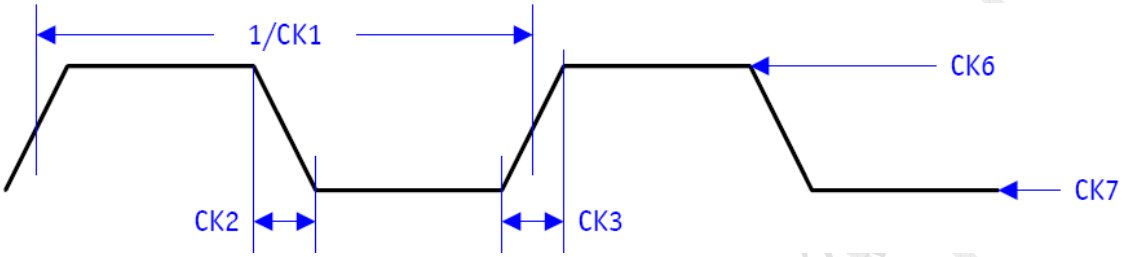


Figure 7-6 WIFI_CLK_32K Input clock timing

Symbol	Description	Min.	Nom.	Max.	Unit
CK1	Frequency	-	32.768	-	kHz
CK2	Fall Time	-	-	100	ns
CK3	Rise Time	-	-	100	ns
CK4	Duty Cycle (High-to-Low Ratio)	15	-	85	%
CK5	Frequency Stability	-50	-	50	ppm
CK6	Input High Voltage				V
CK7	Input Low Voltage				V

<NOTE> WIFI_CLK_32K pin must be grounded when using internal 32KHz clock.

7.3.2 Reference Clock for WLAN

The WIFI reference clock for SWB-A31 is generated from an external clock source frequency of between 19.2MHz and 52MHz (19.2/24/26/38.4/40/52MHz), or an external crystal. The default frequency is 26MHz. Hardware solutions are used for the reference clock as below..

- External crystal option

  <Note> SEMCO recommend the below Crystal (CL=15PF) or equivalent

  ITTI : 14340159-26.000MHz

  SEMCO : SQBD02600Y2QCG / SQ2D02600Y2JCG

  KDS : ZK05956

  NDK : EXS00A-CS04255 (NX2520_26MHz)

- External reference clock option (i.e. XO, VCXO, or VCTCXO)
- Host reference drive option

External Crystal Requirements

Parameter	Min.	Nom.	Max.	Unit
Frequency	-	26	-	MHz
Frequency Stability	-20	-	20	ppm
Effective series resistance (ESR)		-	100	Ohm
● Capacitance (CL)				pF

The external reference clock option or host reference drive option voltage requirements are shown below.

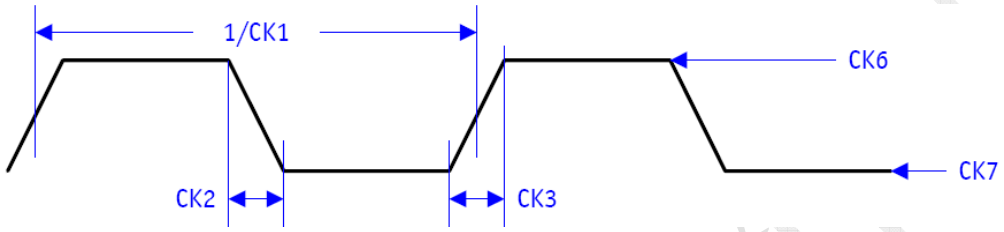


Figure 7-7 External reference clock option or Host reference drive option

Symbol	Description	Min.	Nom.	Max.	Unit
CK2	Fall Time	-	-	0.1*Period	ns
CK3	Rise Time	-	-	0.1*Period	ns
CK4	Duty Cycle (High-to-Low Ratio)	40	-	60	%
CK5	Frequency Stability	-20	-	20	ppm
CK6	Input High Voltage	0.75		3.46	V
CK7	Input Low Voltage				V

When using a TCXO, the clock signal is input at the WIFI_XTALO pin and must be AC-coupled using a 10nF capacitor. The WIFI_XTALI pin must be tied to GND when using a TCXO

7.3.3 Sleep clock for Bluetooth

The sleep clock is an externally provided 32.768KHz clock that is used during deep sleep and in other low-power modes.

Description	Min.	Nom.	Max.	Unit
Frequency	30	32.768	35	kHz
Frequency tolerance		-	250	ppm
Duty Cycle (High-to-Low Ratio)	5:95	50:50	95:5	%
Phase noise	-100 (1KHz offset)			dBc/Hz
	-120 (10KHz offset)			

The sleep clock is only required when BT uses an external reference clock. When the BT uses a crystal oscillator, an external sleep clock is not required.

7.3.4 Reference Clock for Bluetooth

BT_XTALI and BT_XTALO are the pins used for the reference clock. The reference clock is the primary clock source for the SWB-A31 BT section.

Reference clock source may come from either an external crystal or external reference clock source.

Three hardware solutions are used for the reference clock

- External crystal option
- External reference clock option (i.e. TCXO)

External reference clock Requirements

Parameter			Min.	Nom.	Max.	Unit
Frequency			19.2	26	40	MHz
Frequency Stability			-20	-	20	ppm
Duty cycle			30:70	50:50	70:30	%
Edge jitter (at zero crossing)			-	-	1.6	ps rms
Phase noise	F=26MHz	1kHz offset	-	-	-120	dBc/Hz
		10kHz offset	-	-	-130	
		100kHz offset	-	-	-135	
Signal level	AC coupled sinusoidal		200		VDD_ANA	mV pk-pk
	DC coupled digital	VIL	-	VSS	-	V
		VIH	-	VDD_ANA	-	V

※ VDD_ANA = 1.35V nominal

The external clock can be either a digital level square wave or sinusoidal, and this may be directly coupled to BT_XTALI without the need for additional components. If peaks of the reference clock are either below VSS or above VDD_ANA, it must be driven through a DC blocking capacitor connected to BT_XTALI. (In this mode, ground BT_XTALO)

8 Application Reference Design

8.1 Application schematics for separate WiFi & BT clock (Crystal)

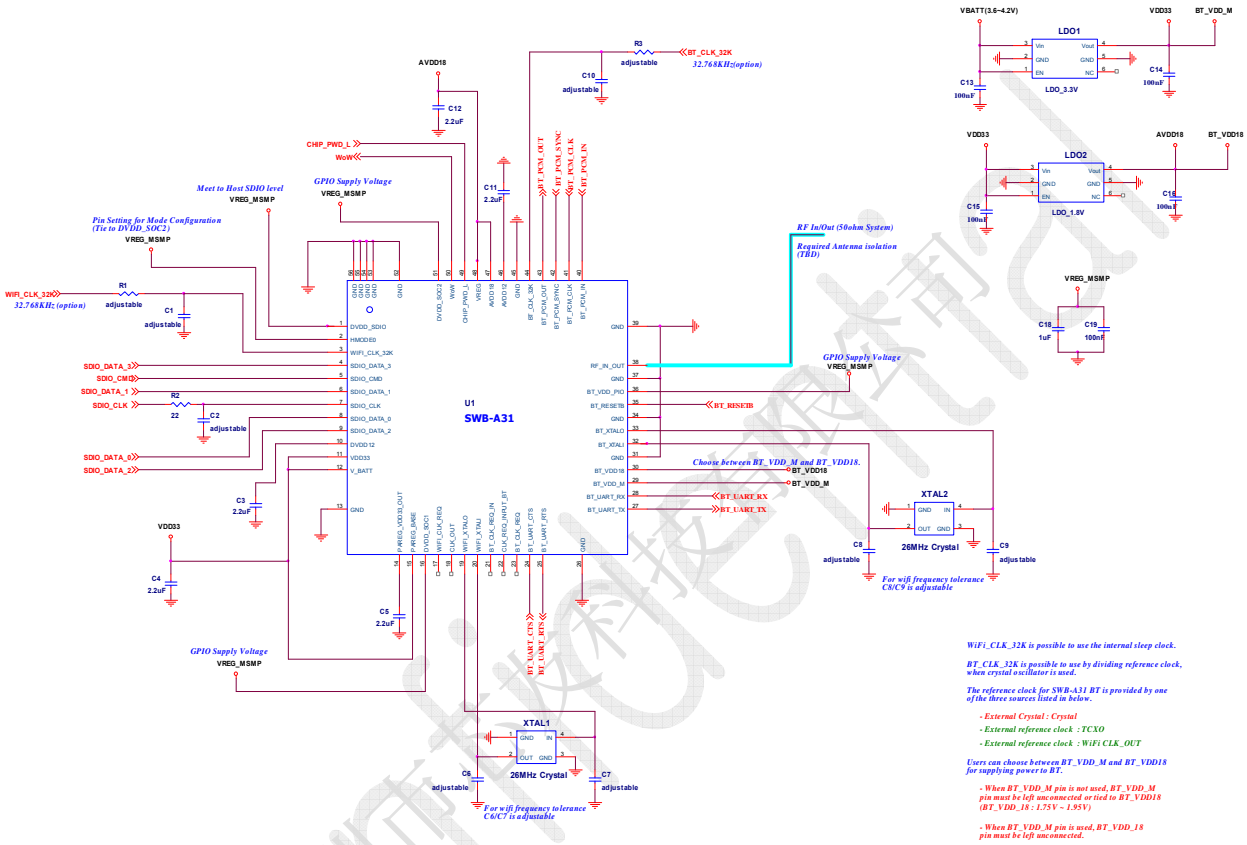
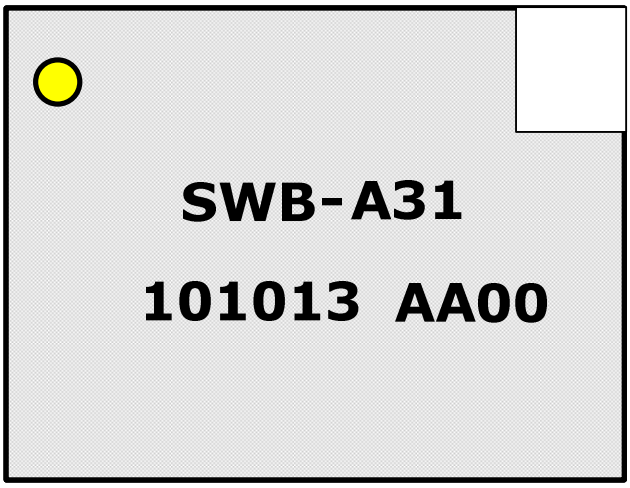


Figure 8-1 Reference Schematic for SWB-A31 Application (separate WiFi & BT ref.clock)

9 Marking Information



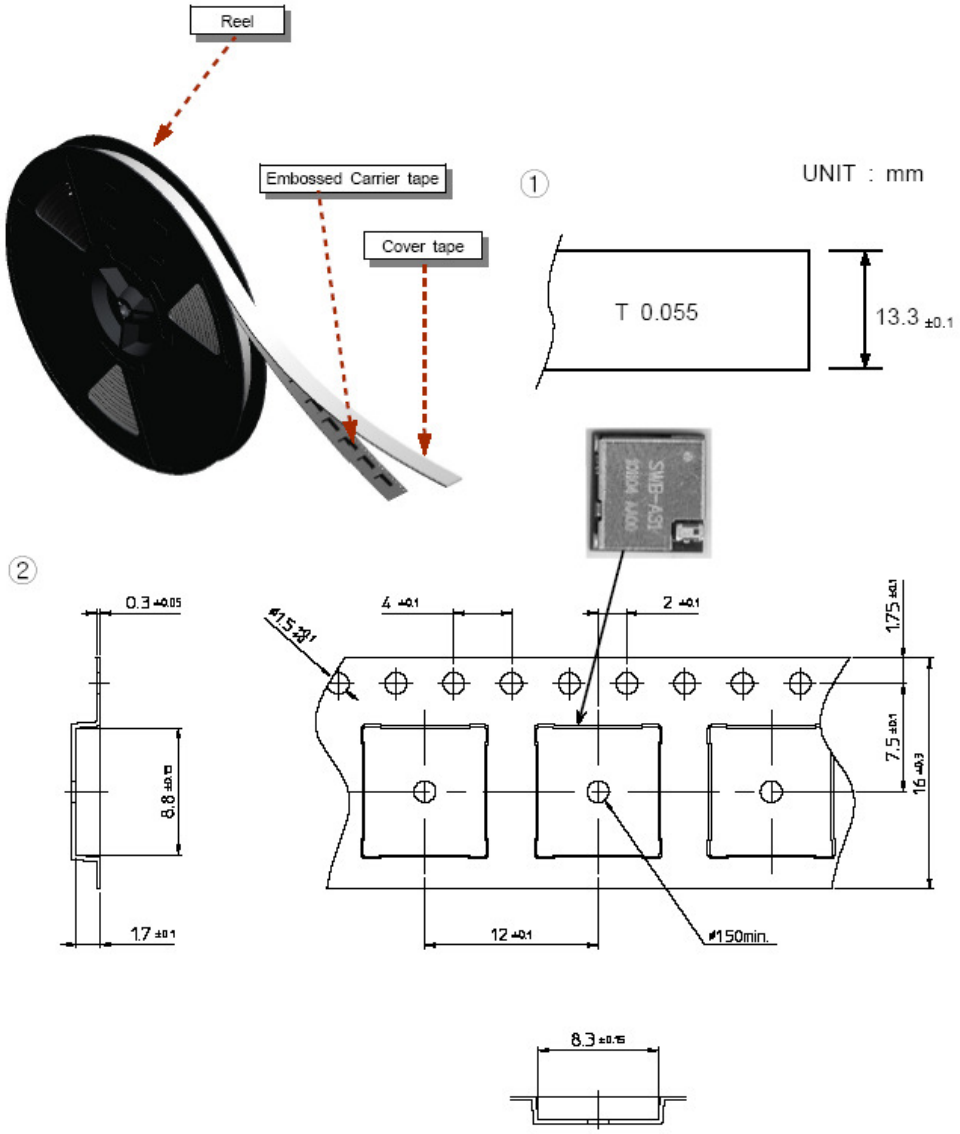
1 0	1 0	1 3		A	A	00
YY	MM	DD		a	b	c

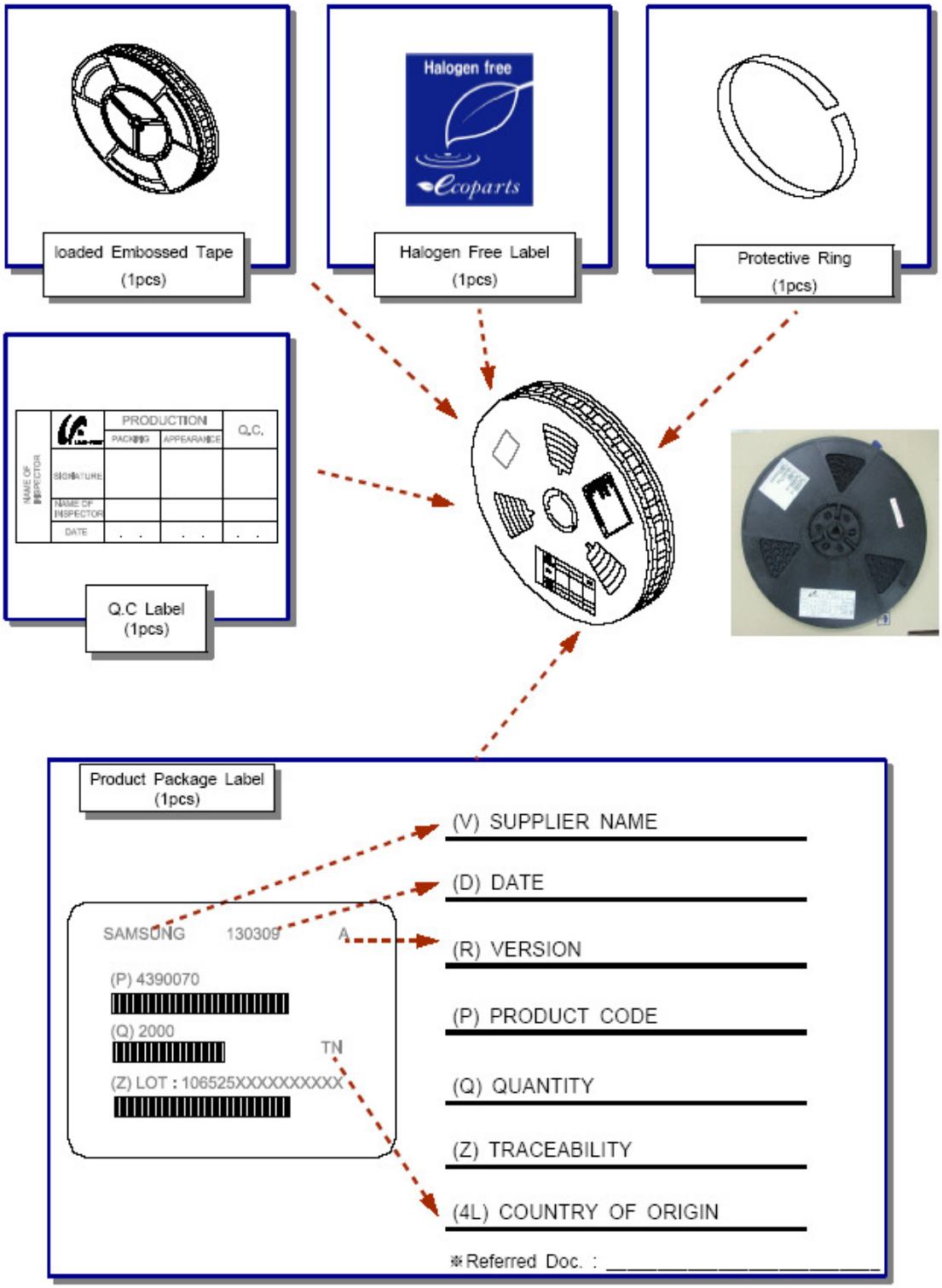
No.	Description
YY	Year: 20XX, XX: 00~99 (ex. 10 = 2010)
MM	Month: XX: 01~12 (ex. 11 = November)
DD	Day: XX: 1~31 (ex. 27: 27st)
a	Manufacture lot
b	Revision information
c	Product subtype code

10 Package Information

10.1 Reel Tape Packing

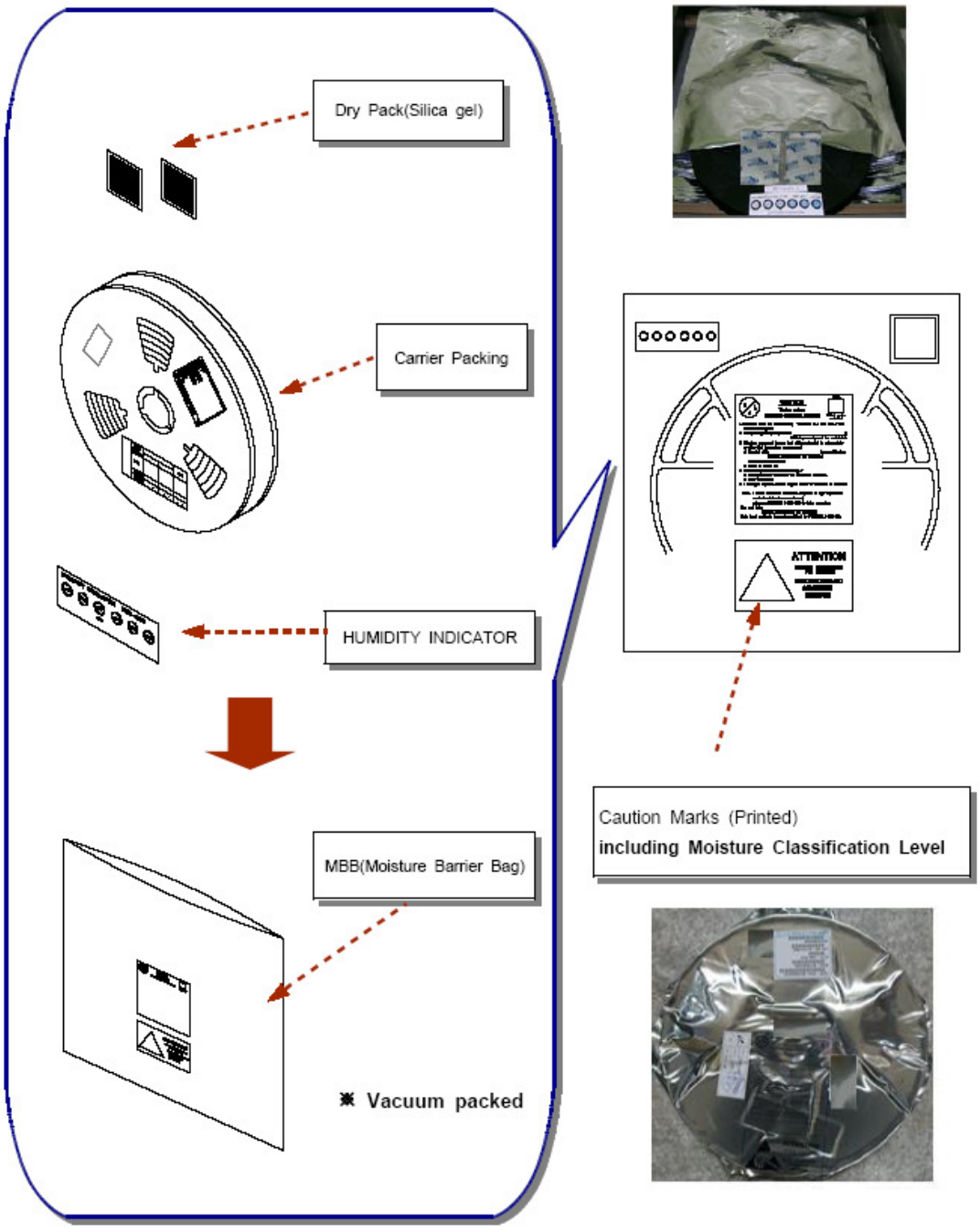
NO	PART NAME	MATERIAL
1	COVER TAPE	PET,ANTISTATIC t0.055
2	EMBOSSED CARRIER TAPE	PS,BLACK,CONDUCTIVE t0.3
	REEL	PS,BLACK,CONDUCTIVE t2.0



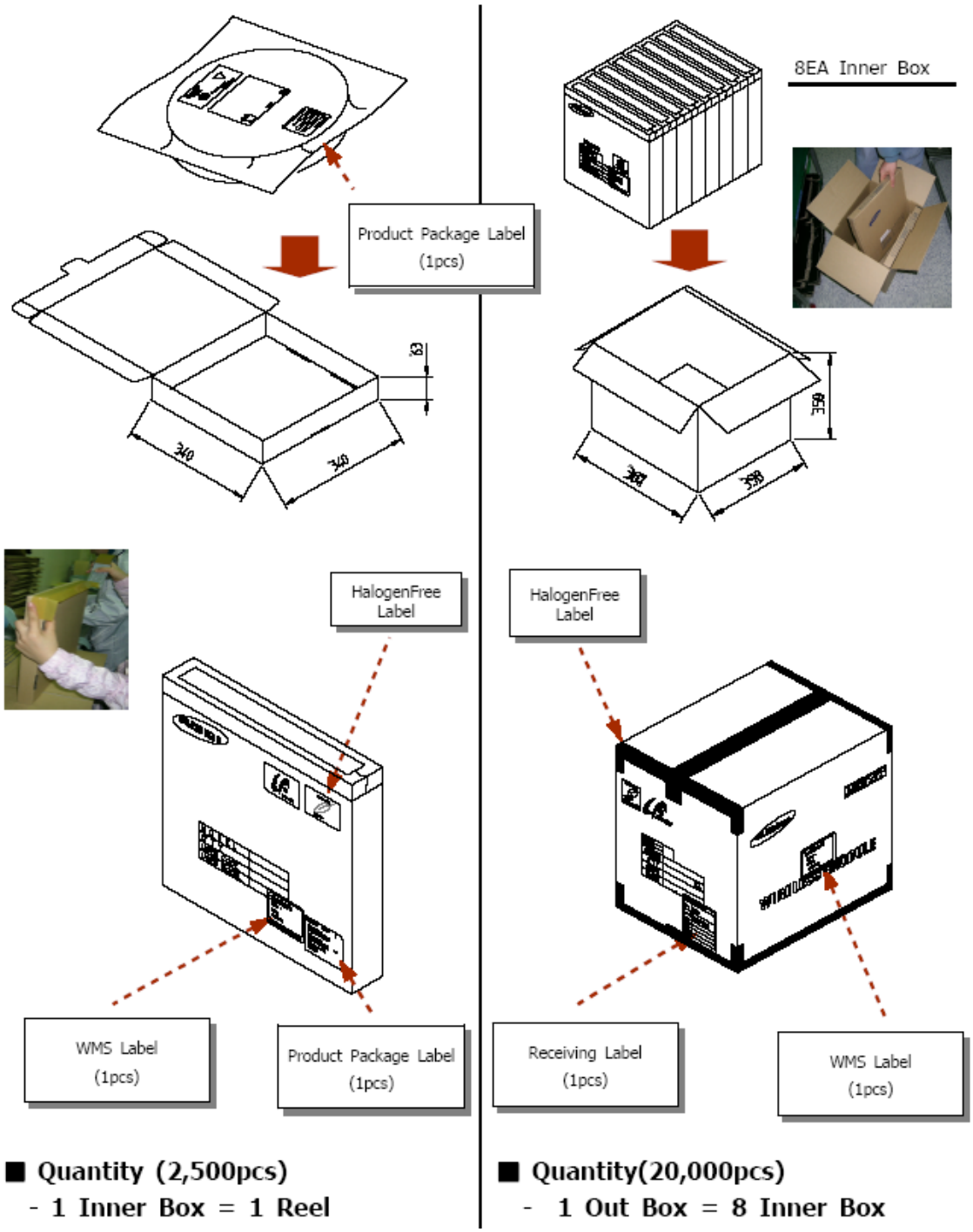

loaded Embossed Tape
(1pcs)
Halogen free
ecoparts
Halogen Free Label
(1pcs)
Protective Ring
(1pcs)
PRODUCTION
PACKING
APPEARANCE
Q.C.
NAME OF INSPECTOR
SIGNATURE
NAME OF INSPECTOR
DATE
Q.C Label
(1pcs)
Product Package Label
(1pcs)
SAMSUNG 130309 A
(P) 4390070
(Q) 2000
TN
(Z) LOT : 106525XXXXXXXXXX
(V) SUPPLIER NAME
(D) DATE
(R) VERSION
(P) PRODUCT CODE
(Q) QUANTITY
(Z) TRACEABILITY
(4L) COUNTRY OF ORIGIN
※Referred Doc. :

10.2 Vacuum Packing

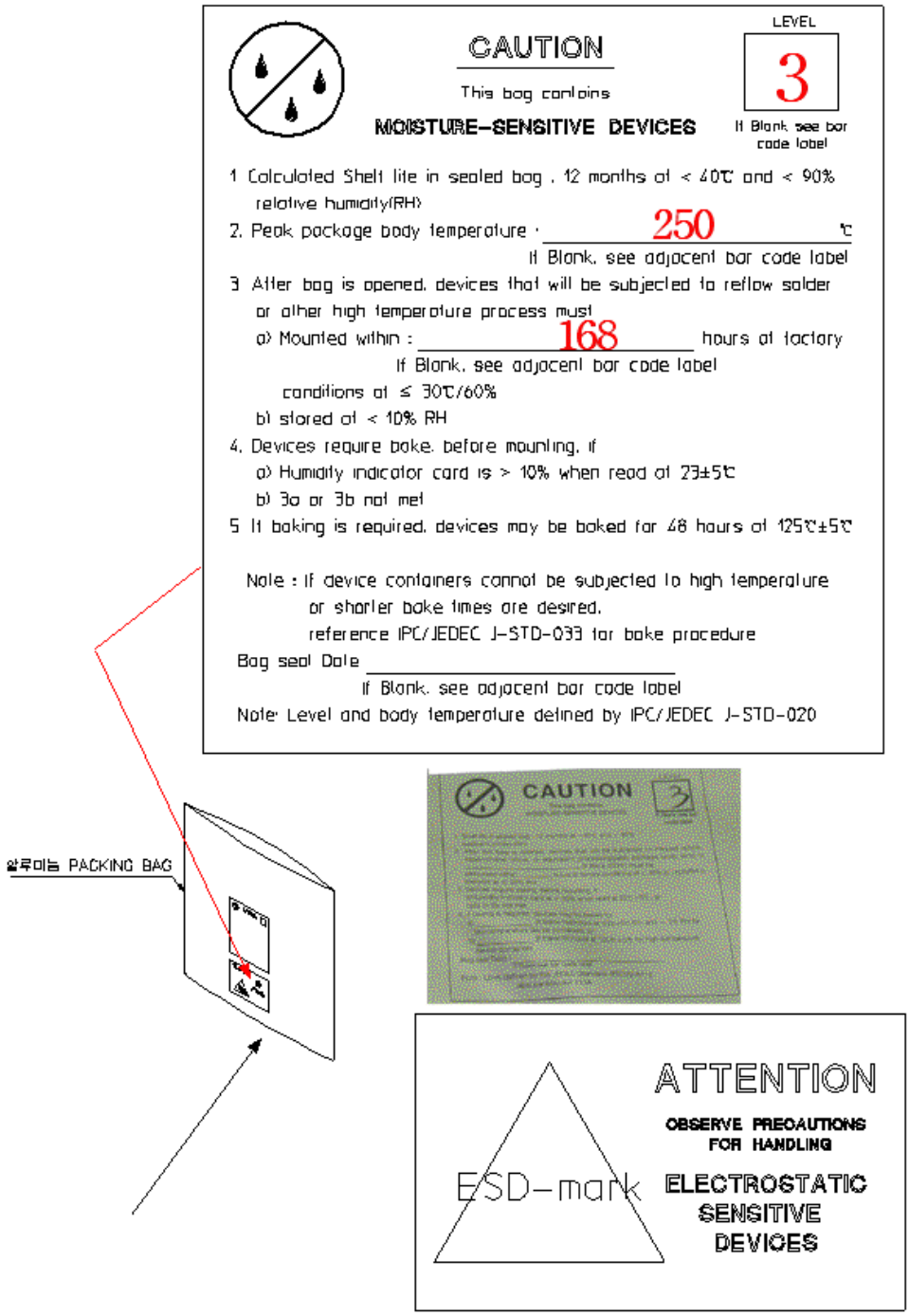
Packed in MBB(Moisture Barrier Bag) and related parts.



10.3 Box Packing



10.4 Shield Bag



10.5 Packing Box ESD Specification

- ESD Control for each packing box : Under 100V
- Packing Box's surface resistance : Max +7 ohms/SQ

11 Handling Moisture Sensitivity

The user must take responsibility during storage and board mount assembly to avoid package overexposure to moisture by following certain precautions explained here.

11.1 Moisture Sensitivity Level

SEMCO follows the latest revision **IPC/JEDEC J-STD-020** standards in determining the module moisture sensitivity level **(MSL)**. To ensure proper SMT assembly, procedures must abide by the MSL and maximum reflow temperature specified on the ESD shipping bag labels.

SWB-A31 is qualified as **MSL 3** and peak package body temperature **250 °C**

11.2 Storage Condition of Moisture Barrier Bag

SWB-A31, as delivered in tape-and-reel carriers, must be stored in sealed, moisture barrier, antistatic bags. Shelf life in a properly sealed bag is 12 months; this specification requires an ambient temperature less than 40 °C and relative humidity less than 90%.

11.3 Out-Of-Bag Duration

After removing from the dry bag, SWB-A31 must be soldered onto the PCB within the time listed on the moisture bag label. SWB-A31 can be exposed for **168 hours** to an environment with a maximum temperature of 30 °C and a maximum relative humidity of 60%, as specified in the **IPC/JEDEC J-STD-033** standard.

11.4 Baking Requirements

Baking prior to solder reflow is required if

- The HIC (Humidity Indicator Card) is > 10% when read at 23 +/- 5 °C, or
- Floor life time (the maximum allowable time period) has been exceeded, or
- Storage condition of < 10% RH has not been met.

For SWB-A31, following baking conditions should be used.

- **Baking condition : 24 hours at 125 °C**

CAUTION: SWB-A31 cannot be baked in the tape-and-reel carriers supplied by SEMCO at the temperature stated on the MSL label.

Revision History

Revision	Date	Descriptions
1	2010-02-11	1st revision
2	2010-10-13	2nd revision Changed BT IC : CSR BC06 => CSR 8810
3	2010-11-24	Changed Section 7.3.1 Sleep clock for WLAN - Add NOTE Changed Section 6.1 - Add example Changed Section 8 Application reference design - PAREG_VDD33_OUT bypass cap : 2.2uF => 2.2uF or 4.7uF Deleted Section 8.2 Application schematics for WiFi & BT clock share
4	2011-01-21	Changed Section 10 Package information